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# HyperLynx PI Power Delivery Network (PDN) Design

**Benefits**

- Automated workflows with HyperLynx's industry-renowned ease of use
- Works with all major PCB layout and routing applications
- Analyze voltage drop due to supply plane copper losses
- Identify areas of excessive current density in layout
- Predict temperature rise with PI/thermal co-simulation
- Analyze power distribution impedance at power supply connections to critical ICs
- Accurate modeling of plane structures for power delivery and noise propagation
- Rapidly explore different stackups, capacitor selections, placements, mounting schemes for their effect on design margins
- Optional PDN Decoupling Optimizer automatically identifies best values & locations for decoupling capacitors

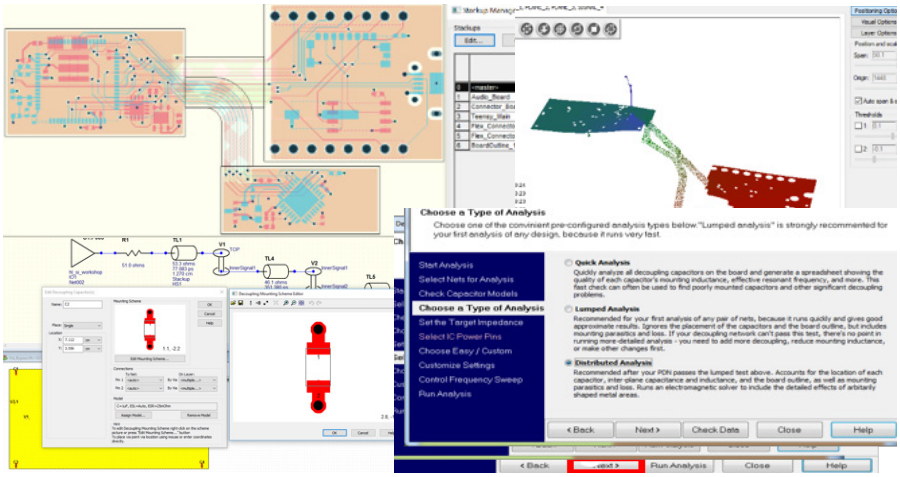
**Overview**

Every modern electronic design includes a Power Distribution Network (PDN) with two critical and equally important purposes:

- Supply stable power to components from DC to ~150 MHz
- Provide controlled return paths for high-speed signals

When a PDN fails to meet these goals, the design can fail to operate at intended performance levels, or even worse, fail intermittently and unpredictably. Poorly designed PDNs can create current and thermal stresses that exceed physical material limits, causing the PCB or ICs to burn out prematurely.

At low (DC) frequencies, resistive losses affect how much current can be supplied to components without excessive drop in supply voltage. Cutouts and voids in power planes increase this effect. Above ~1 MHz (AC), power plane and component pin inductances come into play, limiting how much current can be delivered at these frequencies. Decoupling capacitors provide local reservoirs of charge, but mounting inductances and proximity limit their




HyperLynx PI provides both pre- and post-layout analysis of both DC and AC Power Delivery Network (PDN) behavior. HyperLynx PI lets you maximize design performance and reliability while minimizing both component and manufacturing costs.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# HyperLynx PI Power Delivery Network (PDN) Design

effectiveness. Designing a PDN that meets DC and AC performance requirements is a complex balancing act that requires trading off multiple factors. The use of multiple supply voltages, large dynamic currents, reduced layer counts, increased operating frequencies and smaller noise margins all combine to make good PDN design an exceedingly difficult task.

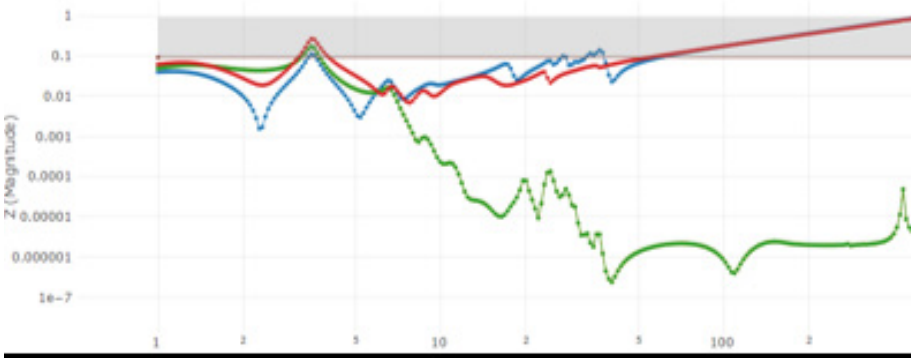
Hardware engineers, PCB designers, and signal integrity specialists alike can use HyperLynx PI to predict PDN performance quickly, without requiring weeks of training. HyperLynx PI identifies power distribution problems early in the design cycle, even prior to layout. Designers identify problems that would be difficult to isolate in the lab, investigating potential solutions using an interactive "what-if" environment. Once layout is complete, HyperLynx PI completely validates PDN behavior as part of electrical sign-off. HyperLynx PI lets you eliminate prototype spins and get to market faster, while creating more reliable and cost-effective designs.

**DC (Voltage Drop) Analysis**
Analyze voltage drop and current density, flag areas where current density exceeds safe limits. Use integrated thermal analysis to identify basic thermal issues or export to FloTherm for detailed thermal modeling. All simulation results are presented in graphical report format, making power delivery problems easy to identify.

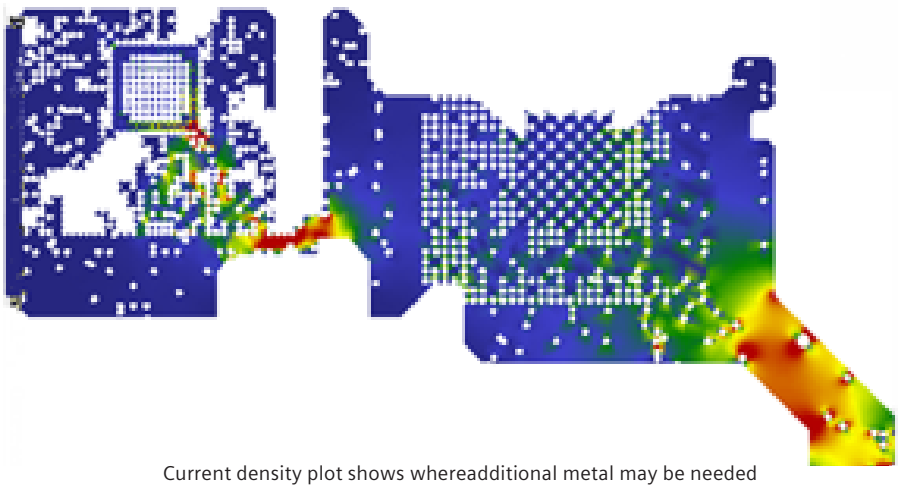
- Fast, high-capacity analysis
- Detailed voltage reporting at component power pins
- Shows 2D and 3D views of voltage distributions
- Plots current density and flow using color to show magnitude
- Export to graphical pre-layout environment for "what-if" analysis on changing copper islands, adding vias, etc.

**AC (Decoupling) Analysis**
Quickly analyze the PDN impedance seen by critical components to ensure it meets requirements. Determine how many capacitors are needed, where to place them and how to mount them. Optimize your design's stackup by investigating the effects of different materials and layer ordering.

- Quickly identify capacitors with large mounting inductance and other connectivity issues
- Best-case analysis establishes minimum decoupling requirements and whether a solution is practical
- Distributed analysis uses integrated 3D EM solver to accurately model complete PDN behavior
- Reports PDN impedance at user-defined locations to ensure critical IC requirements are met
- Exhaustive reports with interactive plots inside the report
- Export layout to graphical pre-layout environment to add/swap capacitors, add vias, etc.




Quickly analyze and display resultsof different decoupling strategies



Current density plot shows whereadditional metal may be needed

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### Pre-Route / What-If Analysis

PDN design isn't complete until the entire board is routed and all DC/AC power requirements are met. HyperLynx PI can be used to perform post-layout power-integrity analysis as soon as critical ICs are placed. When issues arise, possible solutions can be prototyped and evaluated directly in HyperLynx PI without requiring changes to the actual PCB layout (and without requiring changes from the PCB layout designer). HyperLynx PI exports PCB geometries into LineSim for "what-if" analysis. Add or remove copper, change the design stackup, add or remove decoupling capacitors and/or stitching vias – all within the HyperLynx PI environment, using the same easy to use, automated analysis workflows. Once you've identified a potential fix, communicate that back to the PCB designer and import an updated PCB database for verification.

### Optional Decoupling Optimizer

Optimizing decoupling capacitor placement to meet the needs of critical ICs is a multi-dimensional problem that is both detailed and time-consuming. Most designs end up with more decoupling capacitors than they need as a result, to ensure the design has adequate margins. The HyperLynx Decoupling Optimizer automatically determines how capacitors can be eliminated and/or swapped to reduce design costs while still meeting performance targets. Optimization uses a collection of different algorithms to provide multiple tradeoffs between capacitor count, variety and design cost, allowing users to pick the configuration that best meets their unique requirements.

### Supported PCB Layout Systems

- Tightly integrated with Xpedition®, PADS Professional® and PADS®
- Altium Designer (through ODB++)
- Cadence Allegro and OrCAD Layout tools
- Zuken CR Series

### HyperLynx Product Family

HyperLynx PI is part of an integrated family of analysis tools for high-speed electronic design:

- Electrical design rule checking (DRC/ERC)
- Signal integrity analysis (SI)
- Power integrity analysis (PI)
- 3D electromagnetic modeling (3D EM)

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